ecia
Electronic Components Industry Association

Understanding Lead Times

In the realm of modern technology, electronic components stand as the fundamental building blocks powering our digital world. From smartphones to industrial machinery, tiny semiconductor chips, passives, interconnect, and electromechanical devices play an indispensable role in nearly every facet of contemporary life. However, behind their ubiquitous presence, semiconductor production depends on perfect execution of the world's most sophisticated manufacturing processes. Maintaining a balance between manufacturing and global demand is an extraordinarily complex and difficult challenge that often causes extended product cycle time and capacity constraints. This article explains why customers should actively manage their order backlog within the semiconductor supply chain, focusing on the intricate dynamics of manufacturing cycle times, capacity limitations during peak demand, and the nuances across different fabrication (fab) cycle times based on layer count and process technology nodes.

During the pandemic, there was widespread confusion amongst customers about component lead times, how order confirmations could differ, sometimes dramatically, from published lead times. It is critical for customers to understand factors impacting lead times which can vary tremendously, especially in times of tight supply and allocation and use this information effectively to properly manage their backlog. ECIA is attempting to assemble this educational material for customers that explains different factors that affect lead times.

Understanding Semiconductor Product Manufacturing

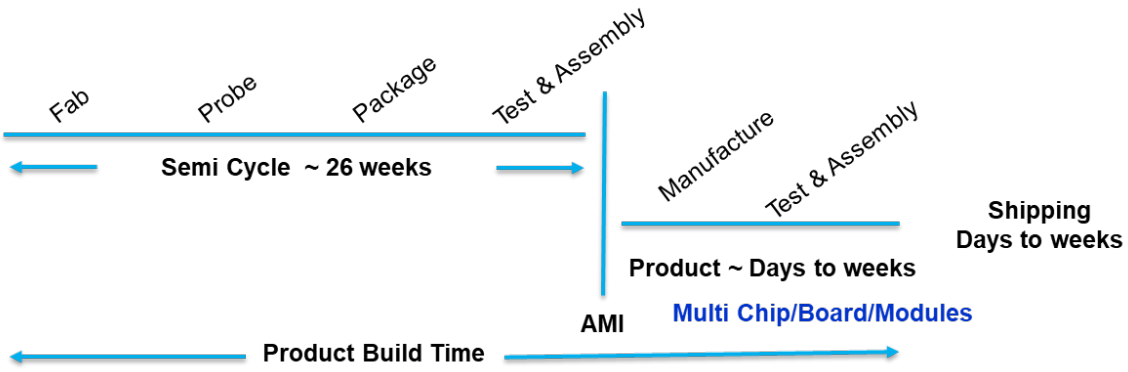
Semiconductor products are "fabricated" on a circular slice of crystalline material (usually silicon) which is referred to as a "wafer". Wafers are batch processed in lots usually consisting of up to 25 wafers. Several identical semiconductor products are printed in a tiled pattern across each wafer. The wafer moves through successive processing recipes (steps) including (but not limited to) photolithography, etch, ion implantation and deposition, to create a pattern of functional electronic devices on the surface of the wafer. The number of steps in the semiconductor manufacturing process varies depending on the complexity of the product. Simple electronic devices such as diodes and discrete transistors can be manufactured with relatively low step counts while high performance processors and high-density memory require high to very high step counts. The semiconductor manufacturing industry commonly refers to "mask layers" as a measure of complexity, where a "mask layer" includes all of the sequential process recipes required to manufacture the product up to the next photolithographic step in the process. Using this nomenclature, the complexity of the semiconductor process can vary from 6-10 mask moves for relatively simple products like discrete diodes and transistors, to 100+ mask layers for the highest performance processors and memory products.

After completion of the "wafer" manufacturing process semiconductor devices must be singulated (referred to as "dicing") and assembled in packages so that they can be accessed. The dicing process involves using a precision saw to separate each tile on the wafer into a separate device. These devices are then assembled in packages which route and connect the semiconductor device to the outside world.

Understanding Semiconductor Manufacturing Cycle Times

Manufacturing cycle times can run from an average of 12 weeks to upwards of 6 months depending on complexity of the fab process, complexity of backend assembly and test, and transportation between steps.

Fab cycle time is the amount of time it takes to process a wafer lot in a fab from start to finish. Wafer fabrication time correlates directly with the complexity of the semiconductor process as mentioned above. Final assembly and test can add an additional 4 to 8 weeks.



The process technology node (typically expressed in nm) refers to the size of the transistors and complexity of the electronic system on the chip. As technology advances, nodes become smaller, enabling more transistors to fit onto a single chip and improving integrated functionality, performance and efficiency. However, smaller nodes often require more advanced and precise manufacturing techniques, thereby potentially increasing the cycle time due to complexity and yield challenges.

Moreover, the number of layers in a semiconductor chip also impacts its manufacturing cycle time. Chips with higher layer counts necessitate more intricate patterning and deposition processes, consequently extending the overall fabrication timeline. For instance, advanced processors designed for high-performance computing or artificial intelligence applications typically have more layers, thus longer cycle times compared to simpler chips like microcontrollers. A 28nm device may have 40 to 50 mask layers. In comparison, a 14nm/10nm device has 60 layers, 7nm 80 to 85, a 5nm device could have 100 layers. Generally, the most common metric for cycle time in the fab is "days per mask layer." On average, a fab takes 1 to 1.5 days to process a layer. So, using today's lithographic techniques, the cycle times are increasing from roughly 40 days at 28nm, to 60 days at 14nm/10nm, to 80 to 85 days at 7nm. 5nm may extend to 100 days using today's techniques, without extreme ultraviolet (EUV) lithography. To complicate matters, the cycle time in the fab increases at the start of a process but drops as the technology matures. During the process, though, cycle times can be impacted by variability issues in the fab. The biggest hit involves the wait times between processing steps.

Capacity Constraints and Peak Demand

Capacity constraints within semiconductor fabs and backend assembly and test facilities present another critical challenge in managing order backlog. Fabs operate at maximum capacity thresholds, dictated by their physical space, equipment capabilities, and workforce availability. During periods of peak demand—often triggered by new product releases, seasonal fluctuations, or geopolitical events—these constraints intensify, leading to potential allocation of manufacturing capacity.

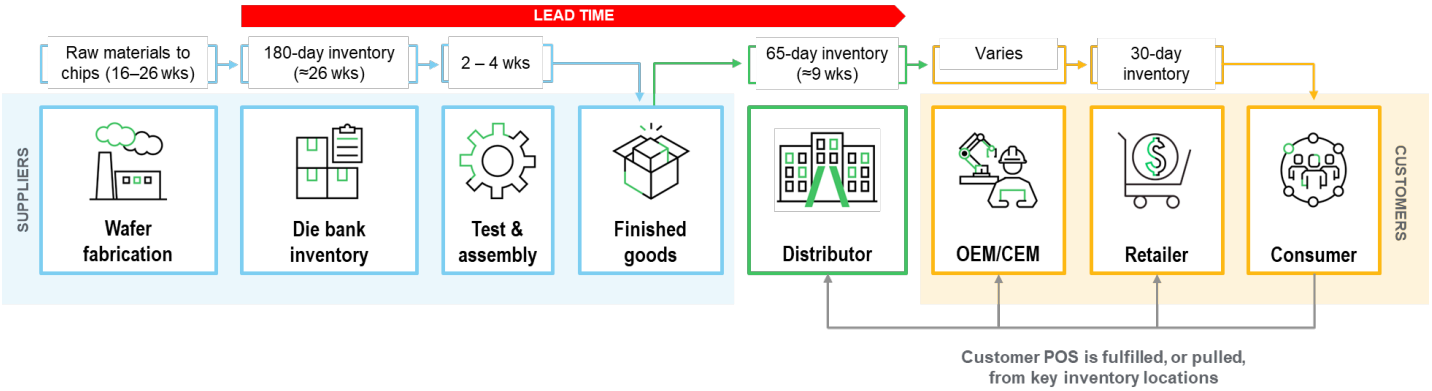
Allocation occurs when semiconductor product demand exceeds manufacturers' supply. During periods of allocation manufacturers generally prioritize certain customers or product lines based on manufacturer's contractual and strategic considerations. This can result in delays for other customers with pending orders, impacting production timelines and ultimately affecting market competitiveness and customer satisfaction. It is important to note that the long term solution to allocation generally requires either significant reconfiguration of manufacturer's capacity, or, more likely, capital investment to increase capacity. Unfortunately, lead time recovery from a period of allocation can take on the order of years when additional equipment and wafer manufacturing clean room facilities are required. Therefore, proactive management of order backlog becomes essential to mitigate such risks and ensure timely and consistent delivery of semiconductor products.

Impact of Inventory

Additional factors can affect lead times, including order quantities and channel choice. Most orders are fulfilled in less time than a full manufacturing cycle due to inventory at different points of the supply chain. For example, small to medium quantities can often be serviced from finished goods inventory in the distribution channel. Authorized distributors are experts at monitoring order patterns, economic conditions, and upstream supply constraints to buffer inventory for their customers. When an order quantity exceeds available distributor stock, orders can often be serviced from a manufacturer's finished goods or die bank (fully completed wafers in storage before dicing), incurring only back-end assembly into packages, final test, and shipping times. If insufficient die bank exists, WIP (work in process) may also allow delivery faster than full cycle times. But large orders, orders of less popular SKU's, or orders for products with no staged inventory points often require full cycle times, fab through backend. And in periods of allocation and fabs running at capacity, fab queue times for wafer starts and increased days per layer in fab can significantly stretch lead times for customers.

Some factors that can affect the lead time to a customer:

- Amount of WIP / Die bank finished wafers in supplier inventory
- Finished inventory on hand with suppliers and/or distributors
- Quantity needed
- Fab allocation time / ownership or outsourcing of wafer fabrication



Importance of Managing Order Backlog

As we approach another upturn in the business cycle, it is imperative that customers understand the effects of lead time variability and properly manage their backlog with their suppliers and distributors. Effective management of order backlog enables customers to navigate the complexities of the semiconductor supply chain more efficiently. By closely monitoring their orders and collaborating closely with semiconductor suppliers and distributors, customers can mitigate supply chain risks, optimize inventory levels, and enhance relationships with suppliers. In conclusion, managing order backlog within the semiconductor supply chain is crucial for navigating the complexities of manufacturing cycle times and capacity constraints. Therefore, customers should prioritize effective backlog management as a cornerstone of their supply chain strategy to compete in today's dynamic global marketplace.